IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, v. STMICROELECTRONICS N.V., STMICROELECTRONICS INTERNATIONAL N.V., and STMICROELECTRONICS, INC, Defendants.	CIVIL ACTION NO. 6:21-CV-00727-ADA JURY TRIAL DEMANDED

PLAINTIFF'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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Plaintiff The Trustees of Purdue University ("Purdue") hereby submits its Responsive Claim Construction Brief addressing the disputed claim terms in U.S. Patent Nos. 7,498,633 (the "'633 Patent") and 8,035,112 (the "'112 Patent") (collectively, the "Asserted Patents"). Additionally, Purdue seeks the exclusion of any testimony from Dr. Vivek Subramanian because Dr. Subramanian is not a person of ordinary skill in the art ("POSITA").

I. INTRODUCTION

Only three terms are at issue:

(1) "a second, thicker oxide layer over said top surface and sidewall of each of said first gate"/ "a gate oxide layer thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates;"[1]

(2) whether the preamble of Claim 9 of the "'633 Patent (reciting a "double-implanted metal-oxide semiconductor field-effect transistor") is limiting; and

(3) "less than about three micrometers."

Defendants ("ST")[2] argued that ***no terms*** required construction in their petitions for *inter partes* reviews ("IPRs"), which were filed against the Asserted Patents in December 2021. According to ST:

> [T]he Board ***need not construe any terms*** of the challenged claims to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a

[1] For the disputed terms of the '112 Patent, Purdue proposes construing the longer phrases, as provided herein, for clarity and context.

[2] Although the opening claim construction brief is purportedly filed only by Defendant STMicroelectronics, Inc. ("ST-INC"), Defendant STMicroelectronics N.V. ("ST-NV") participated in all prior claim construction exchanges. *See* Ex. 1 ("Defendants' Proposed Claim Terms for Construction") at 1; Ex. 2 ("Defendants' Proposed Claim Constructions") at 1; Ex. 3 ("Defendants' Identification of Extrinsic Evidence for Claim Construction") at 1. Moreover, in the IPR petitions, ST-INC identified ST-NV and Defendant STMicroelectronics International N.V. as real parties-in-interest. *See* Dkt. 56-1 at 1; Dkt. 57-1 at 1. Thus, to the extent ST-NV seeks to later take a second bite at the apple on claim construction, Purdue objects.

> POSITA at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.[3]

Dkt. 56-1 at 38-39 (emphasis added); Dkt. 57-1 at 34.

ST now completely reversed itself and contends the terms in question have extraordinary meanings or are indefinite. But ST was correct when it made the representations to the PTAB; for the reasons stated below, none of the terms require construction.

The asserted claims of the '112 Patent are apparatus claims. Nothing in the claim language supports ST's method-based construction for the term "a second, thicker oxide layer over said top surface and sidewall of each of said first gate"/"a gate oxide layer thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates." During the '112 Patent's prosecution, Purdue specifically elected an apparatus claim over a method claim in response to a restriction requirement. *See* Ex. 4 at 8.[4] Thus, ST's attempt to inject a method limitation for making the device layers is wholly improper and effectively attempts to convert the apparatus claims to process claims.

The '633 Patent's preamble ("double-implanted metal-oxide semiconductor field-effect transistor") is not limiting. Contrary to established law, ST improperly looks at the claim elements in isolation. It is indisputable that the '633 Patent relates to silicon-carbide high-voltage semiconductor devices. The patent informs POSITAs what is being claimed without the preamble. *See, e.g.,* '633 Patent, Abstract ("A semiconductor device, such as a metal-oxide semiconductor field-effect transistor"); *id.* at 1:40-57 ("A metal-oxide semiconductor field-effect transistor (MOSFET) may include a semiconductor substrate..."); Dkt. 66 at 15 ("The specification describes

[3] As used herein, the terms "Board" or "PTAB" refers to the Patent Trial and Appeal Board.
[4] All referenced page numbers for the file histories of the Asserted Patents refer to the inserted PDF page numbers on the bottom right.

a number of embodiments, including a MOSFET, double-implanted MOSFET, and vertical double-implanted MOSFET.").

Finally, the use of relative terms, such as "about," do not render patent claims utilizing them indefinite. *See* Dkt. 66 at 16 (arguing "[t]he use of 'less than about three micrometers' to describe the JFET-region width in this limitation renders the claim indefinite because a POSITA cannot determine the upper or lower limits of the numerical range."). Because a POSITA would understand the scope of this term with reasonable certainty, based on the claim language and the specification, this term is not indefinite and need not be construed. *See* Declaration of Dr. Ishwara Bhat ("Bhat Decl."), ¶¶ 31-38.

II. DISPUTED CLAIM CONSTRUCTIONS

A. '112 Patent

1. "a second, thicker oxide layer over said top surface and sidewall of each of said first gate"/ "a gate oxide layer thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates"

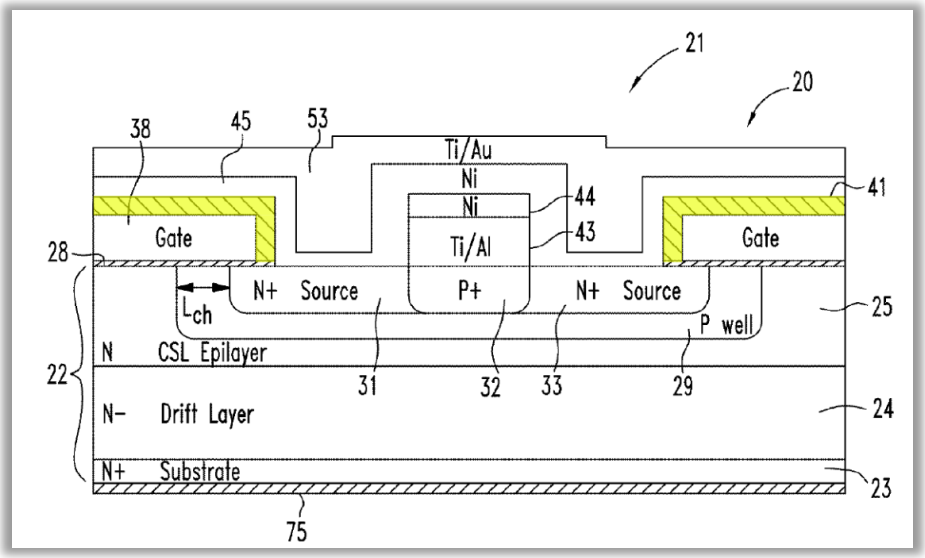
Plaintiff's Proposed Construction	Defendants' Proposed Construction
"layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate"	"an oxidation layer formed, created, or grown by reacting the gate, thicker than the first oxide layer"/ "an oxidation layer formed, created or grown by reacting the gate"

Here, the parties' dispute centers on whether the method of fabrication must be read into the asserted claims. Because claims 1 and 6, reproduced below, are directed to ***products*** and not methods or processes for making the layers at issue, ST's proposal must be rejected.

Claim 1	Claim 6
1. ***A silicon carbide power MOSFET***, comprising: a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof;	6. ***A MOSFET structure***, comprising: a silicon carbide wafer having a substrate body with an upper surface, said substrate body having at least one source region formed adjacent said upper surface;

a plurality of polysilicon gates above said drift layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions, said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region; a first oxide layer between said first gate lower surface and said upper surface of said drift layer; ***a second, thicker oxide layer over said top surface and sidewall of said first gate***; and a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region.	a substrate surface oxidation layer on said upper surface of said substrate body and adjacent said source region; at least two polysilicon gates above said substrate surface oxidation layer, said gates each having a top, a bottom and sides, wherein a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates; ***a gate oxide layer, thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates***; and a material layer over said first source region and between said gate oxide layers on said sides of said gates, said material layer comprising one of an oxide and a metal contact.

In contrast, Purdue's construction is consistent with the claim language and the specification, and even ST admits that Purdue's construction is accurate. *See* Dkt. 66 at 9 ("the disputed terms—'a second, thicker oxide layer' (claim 1) and 'a gate oxide layer' (claim 6)—refer to the layer of oxide that is located over the top and sides of the gates (annotated in yellow in Figure 3 above)"). As shown below, Purdue's construction provides clarity as to the structure of the claimed product itself rather than the process by which it is made, i.e., specifies the position and thickness of each layer.



'112 Patent, FIG. 3 (disputed term highlighted)

Figure 3, a "***power metal-oxide-semiconductor field effect transistor*** (DMOSFET) 21 in accordance with the present invention," and the rest of the specification confirm that Claims 1 and 6 are apparatus claims. '112 Patent at 3:60-63 (emphasis added); *see also id.* at 1:21–23 ("The invention relates generally to semiconductor field effect transistors, and more particularly to field effect transistors having self-aligned source contacts"); *id.*, Front Page ("Sic Power DMOSFET with Self-Aligned Source Contact"). Even ST admits that Purdue's construction is accurate. Dkt. 66 at 9 ("the disputed terms—'a second, thicker oxide layer' (claim 1) and 'a gate oxide layer' (claim 6)—refer to the layer of oxide that is located over the top and sides of the gates (annotated in yellow in Figure 3 above)"); *see also* Bhat Decl. ¶¶ 26-27 (rejecting ST's expert's contention that Purdue's construction is "incorrect" for not specifying the method of making the structure).

Purdue's proposal is further supported by the prosecution history of the '112 Patent, which ST ignores. On September 22, 2010, the Patent Office issued a restriction requirement, requiring the applicant to choose between the product and method claims:

I. Group I, Claims 1-2, drawn to a silicon carbide power MOSFET, classified in class 257, subclass 77.

II. Group II, Claims 3, drawn to a method of fabricating a silicon carbide MOSFET, classified in class 438, subclass 142.

Ex. 4 at 3 (stating that "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the ***product as claimed can be made by another and materially different process***") (emphasis added). And in response, the applicant elected Group I, claim 2, foregoing the method claim, which ST improperly tries to resurrect. *Id.* at 8. Ultimately, Claims 1 and 6 issued from later added and selected claims. *See id*. at 13-16, 25 & 31.

ST's construction is also flawed because it attempts to restrict the claims to a single method of making one particular embodiment, even though the specification makes clear that the fabrication of the claimed products can be accomplished in various ways:

> ***The fabrication of intermediate semiconductor product 58, as shown in FIG. 5, can be accomplished in a variety of ways well known in the art. In one embodiment***, six quarter wafers were processed to produce DMOSFETs in accordance with the present invention, the processing sequence for which is summarized in Appendix I. A detailed run sheet (including materials, temperatures, pressures, times, and chemicals), with slight modifications to the sequence in Appendix I, is provided in Appendix II. ***The method set forth in Appendix I (through step "m") and Appendix II (through step 15 and into step 16) represents one method, with some alternative processing steps, for fabricating the intermediate semiconductor product 58 of FIG. 5***.

'112 Patent at 5:34-46 (emphases added); *see also id.* at 3:2-8 (stating that "no limitation of the scope of the invention is … intended, and that alterations and further modifications in the illustrated device and further applications of the principles of the invention as illustrated therein are contemplated as would normally occur to one skilled in the art to which the invention relates."). Because nothing in the specification or the claim language restricts how the products are made to

the described method, ST's proposed construction should be rejected. *See Info-Hold, Inc. v. Applied Media Techs. Corp*., 783 F.3d 1262, 1267 (Fed. Cir. 2015) (explaining that an invention will only be limited to its preferred embodiment when 'the patentee uses words that manifest a clear intention to restrict the scope of the claims to that embodiment').

Accordingly, the Court should adopt Purdue's construction because it is accurate, consistent with the claims and the specification, and merely provides structural clarity to the apparatus claims at issue. *See U.S. Surgical Corp. v. Ethicon, Inc*., 103 F.3d 1554, 1568 (Fed. Cir. 1997) (declaring "[c]laim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims").

B. '633 Patent

Claim 9, the only asserted claim, recites:

> A double-implanted metal-oxide semiconductor field-effect transistor comprising:
> a silicon-carbide substrate;
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
> a first source region;
> a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
> a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
> a second source region;
> a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
> a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
> a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

1. "double-implanted metal-oxide semiconductor field-effect transistor"

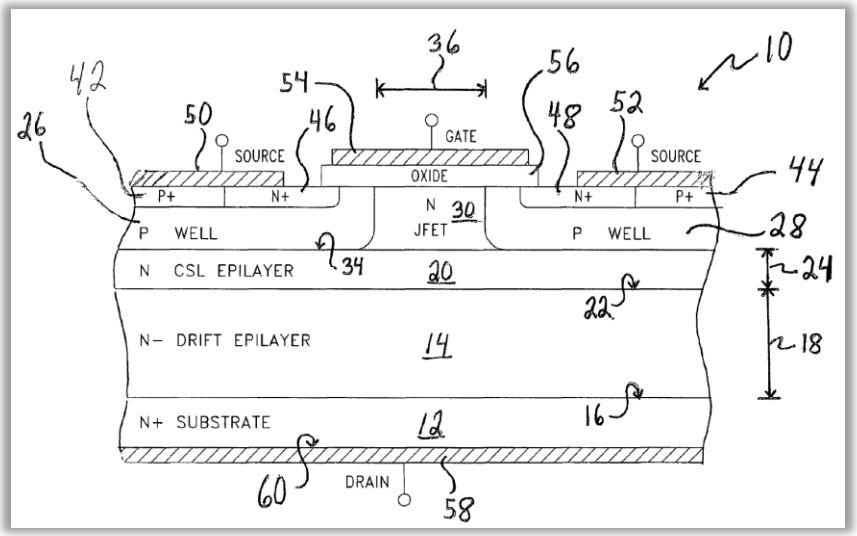
Plaintiff's Proposed Construction	Defendants' Proposed Construction
"The preamble is not limiting"	"The preamble is limiting"

The parties dispute whether the preamble is limiting. A preamble is not limiting unless, upon review of the entire patent, the preamble recites essential structure or steps of the invention. *See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc*., 289 F.3d 801, 808 (Fed. Cir. 2002) ("Whether to treat a preamble as a limitation is a determination resolved only on review of the entire ... patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim.") (internal quotation marks, brackets, and citation omitted); *Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc*., 98 F.3d 1563, 1572–73 (Fed. Cir. 1996) (stating that whether the preamble constitutes a limitation "is determined on the facts of each case in light of the overall form of the claim, and the invention as described in the specification and illuminated in the prosecution history").

Here, the preamble is not "essential" to understanding the claim body based on the entirety of the '633 Patent. Bhat Decl. ¶¶ 28-30. Indeed, it is undisputed that the '633 Patent, titled "High-Voltage Power Semiconductor Device," "relates generally to semiconductor devices, and more particularly to semiconductor devices for high-voltage power applications." '633 Patent at 1:12-13; *see also id*., Abstract ("A semiconductor device, such as a metal-oxide semiconductor field-effect transistor, includes a semiconductor substrate, a drift layer formed on the substrate, a first and a second source region, and a JFET region defined between the first and the second source regions.").

The specification describes various MOSFETs. *See, e.g., id.* at 1:40-2:15 ("A metal-oxide semiconductor field-effect transistor (MOSFET) may include a semiconductor substrate … The MOSFET may also include a first source region, a second source region, and a junction field-effect transistor (JFET) region defined therebetween…"); *id.* at 2:16-3:40 ("The MOSFET may further comprise a plurality of base contact regions formed in each of the first and the second source

regions…The MOSFET may be a double-implanted MOSFET (DMOSFET). For example, the MOSFET may be a vertical DMOSFET…"). And Figure 1 further illustrates the structure of the high-voltage semiconductor device, as shown below.



'633 Patent, FIG. 1

See also '633 Patent at 4:4-12 (not limiting the semiconductor device to a vertical double implanted metal-oxide semiconductor field-effect transistor and stating that it "may be embodied as other types of MOSFET devices."). Based on the foregoing, the device type and structure, including the configuration of the various elements is fairly apparent.

A POSITA would also understand that Claim 9 is directed to a double-implanted semiconductor device, without the preamble, based on the claim elements. Specifically, (1) "a ***plurality of first base contact regions*** defined in the first source region, each of the ***plurality of first base contact regions*** being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode" and (2) "a ***plurality of second base contact regions*** defined in the second source region, each of the ***plurality of second base contact regions*** being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode." '633 Patent, Claim 9 (Emphasis added); Bhat Decl. ¶ 30. Based on the

claim language, a POSITA would know that the second implant is the plurality of the base contact regions defined in the first implant which is the source region. Thus, ST's argument that the preamble is necessary to distinguish a double-implanted from a non-double-implanted device is meritless.[5]

2. "less than about three micrometers"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, no construction necessary.	Indefinite

In its opening claim construction brief, ST completely ignores Purdue's proposed construction for this term — "plain and ordinary meaning, no construction necessary." Because ST was informed of Purdue's amended construction well before the deadline to meet and confer on claim construction, any arguments related to Purdue's previously proposed construction ("about three micrometers or less") should be disregarded. *See* Ex. 5 (clarifying that the plain and ordinary meaning of this term ***is not*** "about three micrometers or less").

More importantly, this term is not indefinite and needs no construction for the following reasons. First, ST conceded as much in its IPR petitions where it professed to have no problem understanding this term (and all other disputed claim terms) and expressly urged adoption of the term's plain and ordinary meaning:

> [T]he Board ***need not construe any terms*** of the challenged claims to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their ***plain meaning*** (as would have been understood by a POSITA at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.

[5] Additionally, the preamble does not provide antecedent basis for a single claim element. For this additional reason, it is not limiting.

Dkt. 56-1 at 38-39 (emphases added); Dkt. 57-1 at 34. ST not only understood "the upper or lower limits of the numerical range" of this limitation, but also repeatedly applied it to the prior art. In fact, ST argued that "Ryu discloses that the JFET region 21 may have a width of less than about three micrometers because the recited width of '***less than about three micrometers' is disclosed with sufficient specificity by Ryu's disclosure of a JFET width 'from about 1 [micrometer] to about 10 [micrometers]***.'" Dkt. 56-1 at 80 (emphasis added); *see also id*. at 78 ("Ryu's 'JFET region' is disclosed as having a range of width that substantially overlaps with the range of 'less than about three micrometers.'").

Second, terms of approximation like "about" or "at least about" are ubiquitous in patent claims, and the Federal Circuit has repeatedly confirmed that they are acceptable and do not render patent claims indefinite. *See, e.g.*, *Ecolab, Inc. v. Envirochem, Inc.*, 264 F.3d 1358, 1367 (Fed. Cir. 2001) ("We note that like the term "about," the term "substantially" is a descriptive term commonly used in patent claims to "avoid a strict numerical boundary to the specified parameter."); *see also Novartis Pharma. Corp. v. Apotex*, 2006 WL 626058, at *10 (S.D.N.Y. Mar. 13, 2006) ("A patent is not invalid merely because claims approximate certain values within it."). Consistent with Purdue's construction, the Federal Circuit has also confirmed that the word "about" should usually be given its ordinary meaning of "approximately." *Merck & Co., Inc. v. Teva Pharms. USA, Inc*., 395 F.3d 1364, 1369 (Fed. Cir. 2005).

Because "it is rarely feasible to attach a precise limitation to 'about,"' this qualifying language generally must "be understood in light of the technology embodied in the invention." *Modine Mfg. Co. v. United States ITC*, 75 F.3d 1545, 1554 (Fed. Cir. 1996), abrogated in nonrelevant part by *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 234 F.3d 558 (Fed. Cir. 2000) (en banc); *see also TransWeb, LLC v. 3M Innovative Properties Co*., No. CIV.A. 10-

4413 GEB, 2011 WL 5825782, at *8 (D.N.J. Nov. 16, 2011) ("At least about" means "at least approximately" and approximately means "within the range of experimental error a person of skill in the art would expect when he/she uses the test methodology described in the patent."). In this case, a POSITA would interpret "about" as implying ±10% variation when referring to a numerical value. Bhat Decl. ¶ 31; *see generally*, '633 Patent (including "about" before specific values). For various reasons, JFET width after fabrication cannot be specified to exact values. *See* Bhat Decl. ¶¶ 32-33 (explaining the well-understood impact of transverse straggle ion implantation species and critical dimension variation during fabrication).

Third, the '633 Patent informs those skilled in the art about the scope of this limitation with ***reasonable certainty***. *Id*. ¶ 38 ("[I]t is my opinion that 'less than about three micrometers,' as used in the context of the '633 Patent, is not indefinite because a POSITA would readily understand the scope of the term with reasonable certainty."); *see also Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 910 (2014) (A claim is indefinite only if, "it "fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention."). ST cannot meet its burden of establishing by clear and convincing evidence that a POSITA "could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area," *Halliburton Energy Serv., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-50 (Fed. Cir. 2008).

Here, the specification clearly provides the relevant range, contrary to ST's assertions. For example, the specification states that "[t]he JFET region may have a width ***less than about three micrometers,***" and further provides that "the JFET may have a width of ***about one micrometer***." '633 Patent at 1:65-67 (emphases added). *See also id*. at 2:47-49; *id*. at 3:26; *id*. at 6:24-27. The purpose of restricting the JFET width is well-understood, i.e., to minimize the area of the unit cell,

thereby increasing the cell density and reducing the on-state resistance. *See* Bhat Decl. ¶¶ 35-36; *see also* '633 Patent at 1:27-33 (stating the specific on-resistance of the semiconductor device is a design consideration, and that "[a]s the specific on-resistance of the device decreases, the efficiency of the semiconductor device may be improved"); *id.* at 6:21-24 ("In some embodiments, the JFET region 30 is also fabricated to have a short width 36 relative to a typical DMOSFET device, which may reduce the specific on-resistance of the semiconductor device 10."); *see also* Bhat Decl. ¶¶ 35-36. A POSITA would understand this purpose. A POSITA would also understand that "less than about 3 micrometers" does not extend down to a width of zero micrometer because that is simply absurd. *Id.*, ¶ 36. Even ST concedes this absurdity. *See* Dkt. 66 at 16 n.8 ("And if the JFET was reduced to zero width, the device would no longer be a …MOSFET.").

Finally, ST's reliance on *Hamilton Products, Inc. v. O'Neill*, 492 F. Supp. 2d 1328 (M.D. Fla. 2007) is misplaced. Unlike in *Hamilton*, as discussed below, ST's expert Dr. Subramanian is not qualified as a POSITA in this case and his opinions should be excluded or given little to no weight. *See* Dkt. at 20 (stating that the court found the expert's testimony persuasive). Further, in *Hamilton*, the inventor's testimony showed intent to read on "all universal" buckles and failed to show the relevant manufacturing tolerances:

> Indeed, it appears that O'Neill has attempted to use assertions of numeric values in describing the dimensions of his buckle to achieve patentability over prior art, but also attempted to use the words "greater than approximately" and "less than approximately" to have his patent read on all universal buckles that function properly. Further, to the extent that O'Neill has asserted that the term "approximately" is used to account for manufacturing tolerances, he has testified that he is unaware of what the limitations of those tolerances would be and has provided no evidence to establish the limitations of such tolerances.

Hamilton, 492 F. Supp. 2d at 1339. That is not the case here. Purdue's expert fully explains some of the reasons for fabrication tolerances in SiC and the specific design goals that affect the JFET

width. Bhat Decl. ¶¶ 32-38; *see also id.* ¶¶ 16-22 (describing the difference between SiC and silicon and their effect on the design of power MOSFETs).

Because a POSITA would understand that "less than about three micrometers" reflects that the numerical value has slight leeway due to processing tolerances, this term requires no construction, and therefore should be afforded its plain and ordinary meaning. *See Bright Sols., Inc. v. Tire Seal, Inc.*, No. CIV. 5:06-CV-247-DF, 2008 WL 5428163, at *20 (E.D. Tex. July 7, 2008), supplemented, No. CIV. 5:06-CV-247-DF, 2008 WL 5429605 (E.D. Tex. Oct. 7, 2008) (construing the term "less than about 500nm" to mean "less than approximately 500 nanometers.").

III. REQUEST TO EXCLUDE DR. SUBRAMANIAN

Purdue asks the Court to strike Dr. Subramanian's opinions or give them little to no weight because he is not qualified as a POSITA. Under *Daubert v. Merrell Dow Pharmaceuticals*, Inc., 509 U.S. 579, 597 (1993), and Federal Rule of Evidence 702, courts are charged with a "gatekeeping role," the objective of which is to ensure that expert testimony admitted into evidence is both reliable and relevant. In patent cases, the Federal Circuit "has explained that only one of ordinary skill in the art who is qualified as a technical expert under Rule 702 of the Federal Rules of Evidence may offer expert testimony on technical matters." *Byrne v. Wood, Herron & Evans, LLP*, 450 Fed. Appx. 956, 962–63 (Fed. Cir. 2011), cert. granted, judgment vacated on other grounds, 568 U.S. 1190 (2013) (citing *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363 (Fed. Cir. 2008)).

In determining whether to exclude an expert based on a lack of requisite scientific, technical, or other specialized knowledge, the court must first define the pertinent art, and what experience and training a person of ordinary skill in the art would have. To define the pertinent art, the court is guided by the language of the Asserted Patents. *Sport Dimension, Inc. v. Coleman*

Co., Inc., No. 14-438, 2015 WL 12732710, at *5 (C.D. Cal. Jan. 29, 2015), *aff'd in relevant part*, 820 F.3d 1316 (Fed. Cir. 2016).

In this case, the pertinent art is the design, fabrication, and operation of high-voltage ***silicon-carbide*** (SiC) semiconductor devices. Dkt. 66-2 ('112 Patent, titled "SiC Power DMOSFET with Self-Aligned Source Contact") asserted claims 1, 6-7, and 10-12; *id.* at 1:50-60 ("SiC power switching devices have significant advantages over silicon devices, including faster switching speed, lower specific on-resistance and thus lower power losses. SiC has a breakdown electric field that is an order of magnitude higher than that of silicon."); *id*. at 2:27-28 ("An intermediate product in the fabrication of a MOSFET, including a silicon carbide wafer"); *id*. at 4:14-22 ("Substrate 23 and the layers and implants are formed from silicon-carbide and doped with N-type or P-type impurities as shown in FIG. 3 and described herein."); Dkt. 66-3 ('633 Patent) asserted claim 9, *id.* at 1:44-45 ("The semiconductor substrate may be formed from a silicon carbide material."); *see also* Bhat Decl. ¶¶ 14-22.

But Dr. Subramanian has ***zero*** experience with SiC devices. *See generally* Dkt. 66-1, ¶¶ 6-12. The fact that he has worked with conventional silicon devices generally (*Id.*, ¶ 6) does not make him an expert on SiC devices because of the inherent differences between the two. *See*, *e.g.*, Dkt. 66-2 at 1:50-53 ("Although silicon has been the material of choice for many semiconductor applications, its fundamental electronic structure and characteristics prevent its utilization beyond certain parameters."); *id*. at 1:55-60 ("SiC power switching devices have significant advantages over silicon devices, including faster switching speed, lower specific on-resistance and thus lower power losses. SiC has a breakdown electric field that is an order of magnitude higher than that of silicon."); Ex. 6 at 9-10, 20-22 (explaining the incompatibility of silicon MOSFET devices with a silicon-carbide substrate, i.e., render the device unsatisfactory or inoperable for its intended

purpose). Because the design considerations for SiC power devices are materially different from those governing the design of silicon power devices, proficiency in the design of silicon power devices does not translate into proficiency in the design of SiC devices. Bhat Decl. ¶¶ 15-22 (discussing the design considerations for SiC power devices and emphasizing that SiC experience is necessary to qualify as a POSITA). And although Dr. Subramanian states that he has "designed and fabricated high voltage ***wide bandgap devices***," none of the publications and patents listed on his CV relate to wide bandgap devices. *See* Ex. 7. More importantly, SiC is never mentioned in any of those publications. Nothing in the materials ST has provided establish their expert has any relevant experience, knowledge, or training in the very specialized types of semiconductor devices at issue.

IV. CONCLUSION

For the foregoing reasons, the Court should adopt Purdue's proposed constructions for the disputed terms, and strike Dr. Subramanian's opinions, or alternatively give them little to no weight.

Dated: March 14, 2022

Respectfully submitted,

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THE TRUSTEES OF PURDUE UNIVERSITY

CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on March 14, 2022, all counsel of record who have appeared in this case are being served with a copy of the foregoing via the Court's CM/ECF system.

/s/ Halima Shukri Ndai
Halima Shukri Ndai